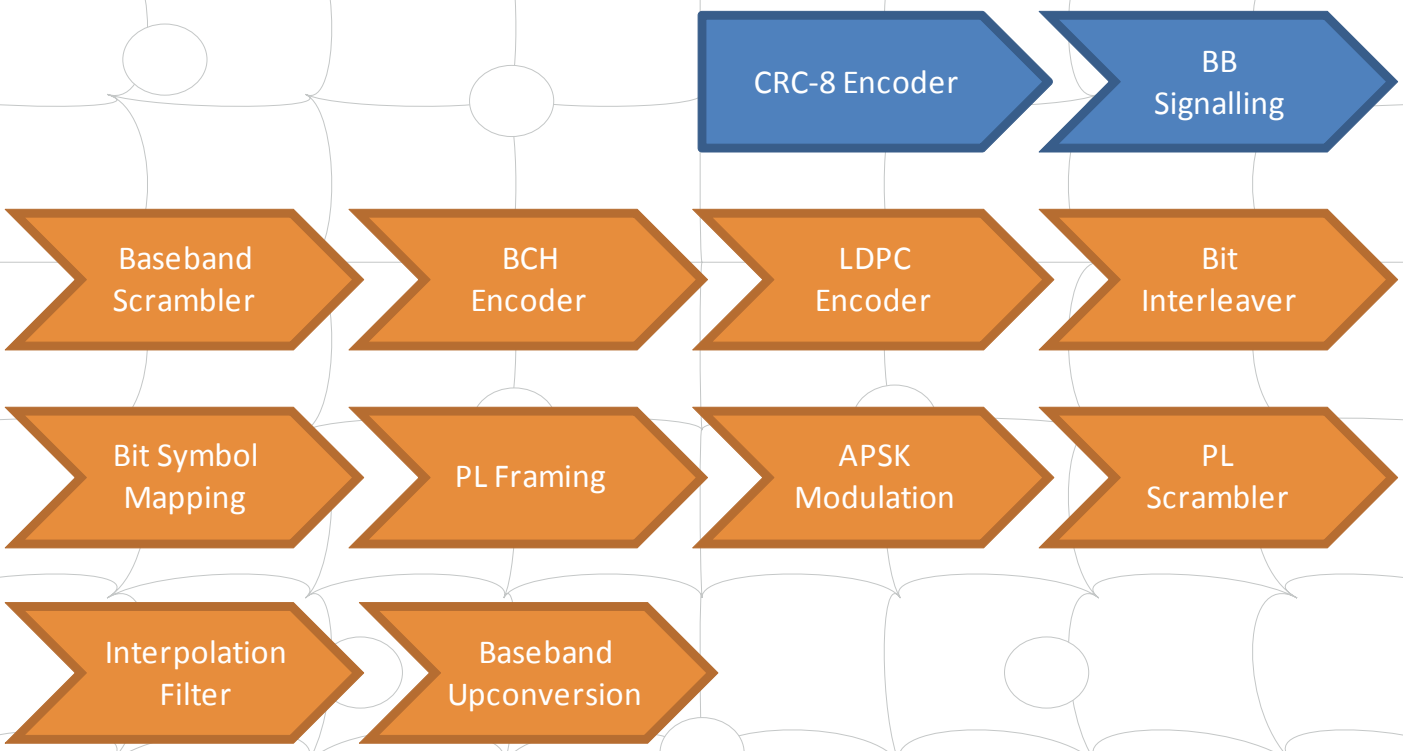

DVB-S2 Modulator FPGA IP-Core

maintech GmbH

DVB-S2 Modulation According to ETSI-EN 302307 V1.2.1

- Constellations: QPSK, 8PSK, 16APSK, 32APSK
- Symbol rate 1-32 MSym/s
- Implementation using a single 27MHz crystal; other frequencies are possible
- Integrated IF upconverter and interpolation filter
- Level correction
- FEC (LDPC): 1/4, 1/3, 2/5, 1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 8/9, 9/10
- TS processing (stuffing packets generator, PCR correction)
- No external dependencies
- In conjunction with the AD9772 DAC (I/Q output) or AD9744 DAC (IF output): >27dB MER

Ressource Requirements

- Altera Cyclone 3 (EP3C40), IF output: ~13200 LEs, 70 blockrams, 69 multipliers
- Xilinx Spartan 3 (XC3SD1800A), I/Q baseband: ~4400 slices, 30 blockrams, 72 multipliers
- Lattice: on request

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IP Core

For custom hardware developments, the use of an IP core offers the chance to save on development time and opens the possibility of using existing hardware in new applications. The maintech DVB-S2 IP core is especially suited for this as it was developed with particular attention on the following aspects:

- Flexible configuration depending on available ressources and necessary RF processing
- Operation with a single 27MHz crystal
- The modulated signal is available as I/Q base-band or alternatively as a ready-to-use IF signal
- A powerful interpolation filter makes sure that any desired DAC sample rate can be used
- The resulting IF can be chosen freely in steps of a few hundred Hertz
- To compensate for the unavoidable FIFO delay, PCR correction and a stuffing packets generator are available which raises the transport stream rate to the needed transmission rate
- All transmission parameters can be changed during operation of the IP core; changes are immediately applied

Licensing

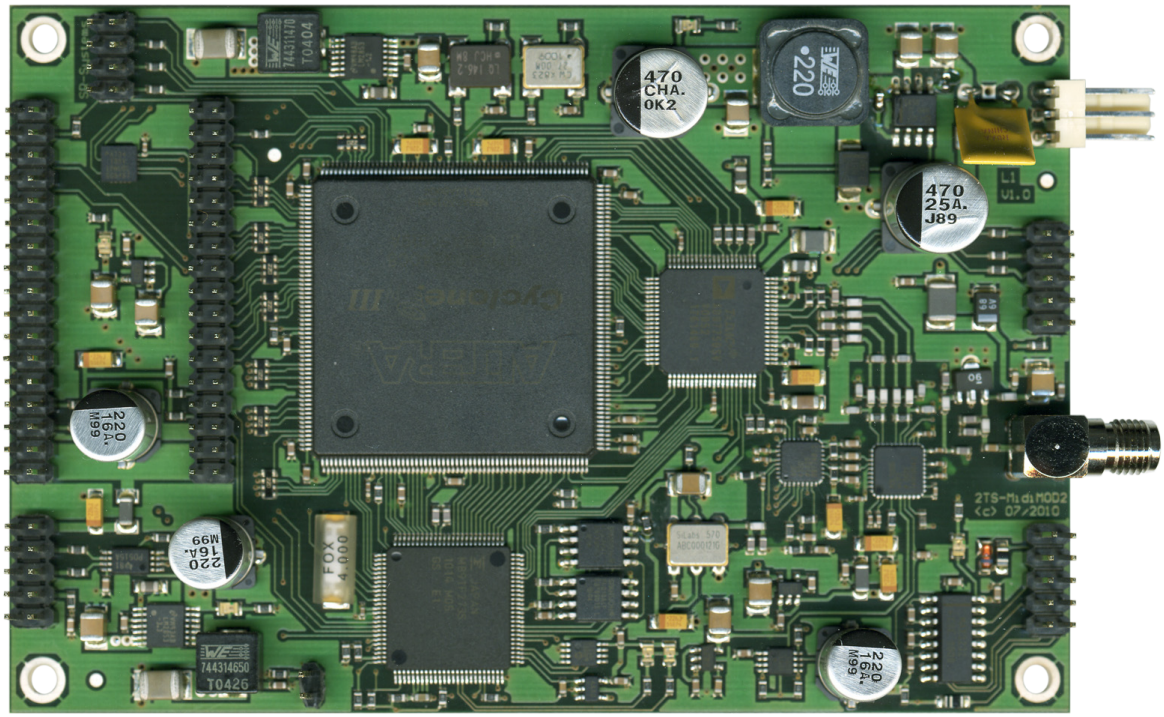
The DVB-S2 IP core is available in different configurations. Depending on your budget and wishes, finished binary images or the complete VHDL source code can be delivered – please contact us for a quote for your planned application.

DVB-S2 Modulation

DVB-S2, follow-up of the DVB-S standard, features a higher transmission capacity at the same bandwidth and transmission power. Not only SDTV but HDTV and H.264 data streams can be transmitted in that efficient mode, too. DVB-S2 modulation can also make sense for the transmission of great masses of data or internet services.

maintech's IP-Core unites all advantages of the DVB-S2 modulation: The IP-Core provides a powerful LDPC error corection, all constellation types as QPSK, 8PSK, 16APSK, 32APSK and the roll off factors 0.2, 0.25 and 0.35

Constellations	QPSK, 8PSK, 16APSK, 32APSK
Symbol rate	1-32 Msym/s in steps of 1ksymbol
MER	>27dB
FEC (LDPC)	1/4, 1/3, 2/5, 1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 8/9, 9/10 (depending on the constellation type)
Roll off factor	0.2, 0.25, 0.35
Pilots	on/off
TS Input	8 Bit parallel + clock & sync (SPI), PCR correction included MPEG2-TS GS available on request
Platforms	Altera, Xilinx, Lattice
Language	VHDL
Dependencies	none



Application example: DVB-S2 Modulator MidiMod from SR-Systems

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