

COFDM Modulator FPGA IP-Core



DVB-T Modulation According to ETSI-EN 300744 V1.5.1

- Constellations: QPSK, QAM16, QAM64
- IFFT Modes: 2k and 8k
- Bandwidth: 6MHz, 7MHz and 8MHz
- Implementation using a single 27MHz crystal
- Integrated IF upconverter and interpolation filter
- IF output adjustable between 3.5MHz and 70MHz
- Level correction down to -10dB
- TS processing (bitrate adaption, PCR correction)
- No external dependencies
- In conjunction with the AD9772 DAC: >40dB MER

Ressource Requirements

- Altera Cyclone 3 (EP3C55), 2k/8k mode, IF output:
~10500 LEs, 87 blockrams, 21 multipliers
- Xilinx Spartan 3 (XC3S400), 2k mode, I/Q baseband:
~3000 slices, 12 blockrams, 16 multipliers
- Lattice ECP3 (LFE3-70E), 2k/8k mode, IF output:
~7400 slices, 44 blockrams, 31 multipliers

maintech GmbH
Max-Planck-Str. 8
D-97204 Höchberg
Germany

Tel +49-(0)931-4070690
Fax +49-(0)931-4070653

Mail info@maintech.de
Web www.maintech.de

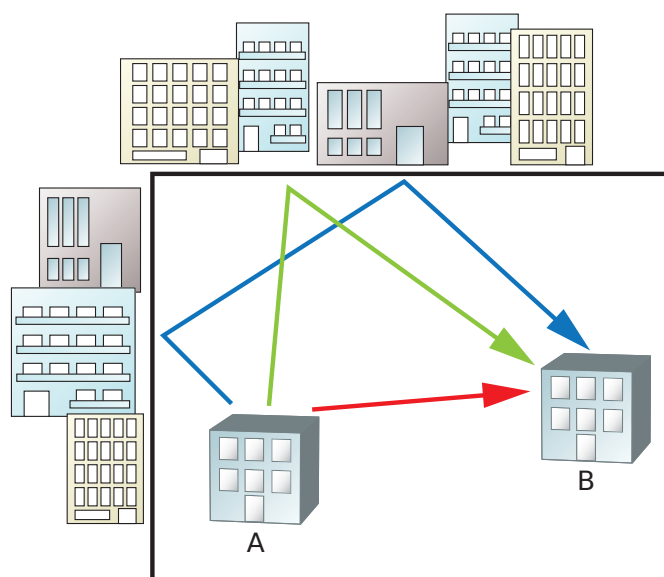
COFDM Benefits

Contrary to the established DVB variants DVB-S and -C, DVB-T does not use a single carrier but up to 6817 orthogonal carriers. Each one of these carriers is modulated with QAM64 at most.

Since these carriers are modulated at a much lower rate, the resulting symbol duration of about 1ms is much longer. Opposing to DVB-S where a few meters difference of propagation distance result in catastrophic inter-symbol-interference, DVB-T can handle many kilometers without problems.

According to this, DVB-T is especially suited to be used in the following environments:

- Areas densely covered with buildings causing a lot of reflections on house walls etc.
- Mountainous regions
- Inside buildings



DVB-T Datapath

The main difference in the internal datapath of DVB-T compared to the other DVB variants is the implementation of a much more powerful forward error correction scheme.

The transmission is based on the standardised ISO/IEC13818-1 MPEG2 transport stream which specifies the multiplexing of audio, video and management data in packets of 188 bytes size.

After adding the Reed-Solomon error correction code, which prolongs the packets from 188 bytes to 204 bytes, several additional steps of convolutional coding and interleaving are performed. These steps make sure that neither single obstructed carriers nor short burst errors result in corrupted payload.

These error correction algorithms can be configured to match the working environment perfectly - the resulting datarates are in the range between 4.9MBit/s and 31.6MBit/s at a RF bandwidth of 8MHz.

IP Core

For custom hardware developments, the use of an IP core offers the chance to save on development time and opens the possibility of using existing hardware in new applications.

The maintech COFDM IP core is especially suited for this as it was developed with special attention on the following aspects:

- Flexible configuration depending on available resources and necessary RF processing
- Operation with a single 27MHz crystal
- The modulated signal is available as I/Q baseband or alternatively as a ready-to-use IF signal
- A powerful interpolation filter makes sure that any desired DAC sample rate can be used
- The resulting IF can be freely chosen in steps of a few hundred Hertz
- To compensate for the unavoidable FIFO delay, a stuffing generator and PCR correction is available which raises the transport stream rate to the needed transmission rate
- All transmission parameters can be changed during operation of the IP core; changes are immediately applied
- Non-standardised datarates and bandwidths are possible

Constellations	QPSK, QAM16, QAM64
FEC	1/2, 2/3, 3/4, 5/6, 7/8
Guard Intervals	1/4, 1/8, 1/16, 1/32
IFFT Modes	2k or 8k (8k optional)
Bandwidth	1MHz to 8MHz
IF Output	I/Q baseband or continuous between 3.5MHz and 70MHz
Level correction	0dB down to -10dB
TS Input	8 Bit parallel + clock & sync (SPI), PCR correction included
Platforms	Altera, Xilinx, Lattice
Language	VHDL
Dependencies	none

Licensing

The COFDM IP core is available in different configurations. Depending on your budget and wishes, finished binary images or the complete VHDL source code can be delivered – please contact us for a quote for your planned application.