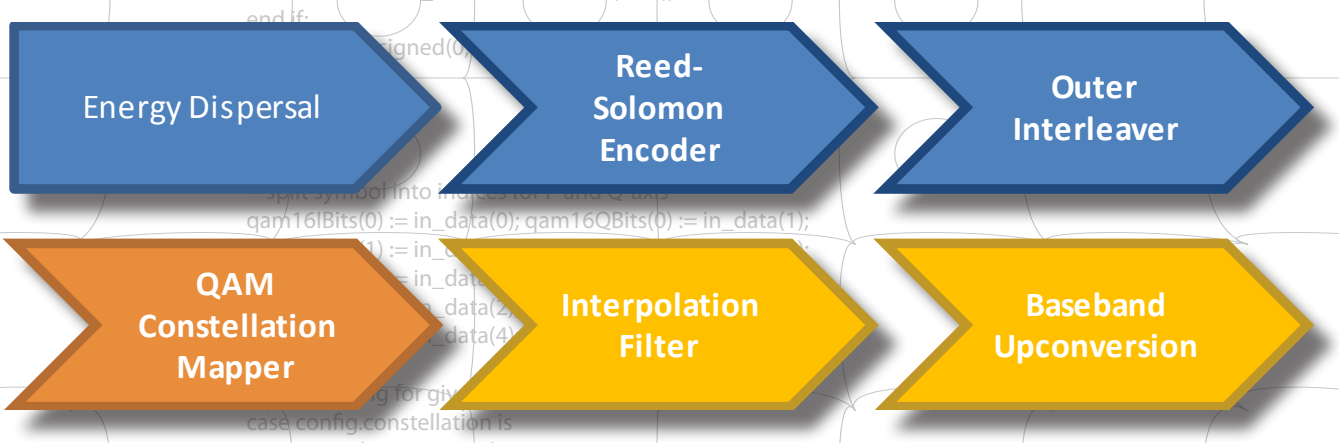

QAM Modulator FPGA IP-Core

maintech GmbH

DVB-C Modulation According to ETSI-EN 300429 V1.2.1

- Constellations: QAM16, QAM32, QAM64, QAM128, QAM256
- Symbol rate: 1000-7000 ksym/s
- Implementation using a single 27MHz crystal
- Integrated IF upconverter and interpolation filter
- IF output adjustable between 3.5MHz and 70MHz
- Level correction down to -10dB
- TS processing (bitrate adaption, PCR correction)
- No external dependencies
- In conjunction with the AD9772 DAC: >40dB MER

Ressource Requirements

- Altera Cyclone 3 (EP3C55), IF output:
  ~6000 LEs, 9 blockrams, 33 multipliers
- Xilinx Spartan 3 (XC3S400), I/Q baseband:
  ~1700 slices, 1 blockram, 16 multipliers

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IP Core

For custom hardware developments, the use of an IP core offers the chance to save on development time and opens the possibility of using existing hardware in new applications.

The maintech QAM IP core is especially suited for this as it was developed with special attention on the following aspects:

- Flexible configuration depending on available ressources and necessary RF processing
- Operation with a single 27MHz crystal
- The modulated signal is available as I/Q baseband or alternatively as a ready-to-use IF signal
- A powerful interpolation filter makes sure that any desired DAC sample rate can be used
- The resulting IF can be freely chosen in steps of a few hundred Hertz
- To compensate for the unavoidable FIFO delay, a stuffing generator and PCR correction is available which raises the transport stream rate to the needed transmission rate
- All transmission parameters can be changed during operation of the IP core; changes are immediately applied

Licensing

The QAM IP core is available in different configurations. Depending on your budget and wishes, finished binary images or the complete VHDL source code can be delivered - please contact us for a quote for your planned application.

Constellations	QAM16, QAM32, QAM64, QAM128, QAM256
Symbol rate	1000-7000 ksym/s
MER	>40dB
IF Output	I/Q baseband or continuous between 3.5MHz and 70MHz
Level correction	0dB down to -10dB
TS Input	8 Bit parallel + clock & sync (SPI), PCR correction included
Platforms	Altera and Xilinx
Language	VHDL
Dependencies	none

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