

DVB-C2 Modulator FPGA IP-Core

DVB-C2 Modulation according to ETSI-EN 302 769 V1.2.1

- · Constellations: QPSK, 16QAM, 64QAM, 256QAM, 1024QAM, 4096OAM
- FEC (LDPC): 2/3, 3/4, 4/5, 5/6, 8/9, 9/10
- Frequency Interleaver incl., Time Interleaver optionally
- · Number of dataslices: only limited by FPGA size
- Bandwidth: freely selectable, only limited by FPGA size
- Channel spacing: 6, 8 MHz
- TS processing (stuffing packets generator, PCR correction)
- Output: Baseband, IF or target frequency (optionally)
- MER >40dB (depending on the DAC)
- Implementation using a single crystal
- No external dependencies

Ressource Requirements

· Altera, Xilinx or Lattice; information on request

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IP Core

For custom hardware developments, the use of an IP core offers the chance to save on development time and opens the possibility of using existing hardware in new applications. The maintech DVB-C2 IP core is especially suited for this as it was developed with particular attention on the following aspects:

- Flexible configuration depending on available ressources and necessary RF processing
- Operation with a single 27MHz crystal
- The modulated signal is available as I/Q baseband or alternatively as a ready-to-use IF signal
- A powerful interpolation filter makes sure that any desired DAC sample rate can be used
- The resulting IF can be chosen freely in steps of a few hundred Hertz
- To compensate for the unavoidable FIFO delay, PCR correction and a stuffing packets generator are available which raises the transport stream rate to the needed transmission rate
- All transmission parameters can be changed during operation of the IP core; changes are immediately applied

DVB-C2 Modulation

DVB-C2, follow-up of the DVB-C standard, is based on COFDM modulation. DVB-C2 features a higher transmission capacity at the same bandwidth and transmission power. Not only SDTV but HDTV and H.264 data streams can be transmitted in that efficient mode, too. DVB-C2 modulation can also make sense for the transmission of great masses of data or internet services.

maintech's IP-Core unites all advantages of the DVB-C2 modulation: The IP-Core provides a powerful LDPC error corection and features all constellation types as QPSK, 16QAM, 64QAM, 256QAM, 1024QAM as well as 4096QAM.

Apart from DVB-T, DVB-C and DVB-S IP-Cores there are also IP-Cores for DVB-S2 and DVB-T2 available. You'll find further information on www.maintech. de.

Licensing

The DVB-C2 IP core is available in different configurations. Depending on your budget and wishes, finished binary images or the complete VHDL source code can be delivered – please contact us for a quote for your planned application.

Input	 Single TS per dataslice 8 Bit parallel + clock & sync (SPI) Rate adaptation incl. PCR correction (optionally) GSE / BBFRAME input on request
Constellations	QPSK, 16QAM, 64QAM, 256QAM, 1024QAM, 4096QAM
FEC (LDPC)	2/3, 3/4, 4/5, 8/9, 9/10 (depending on the constellation type)
Interleaving	 Bit interleaver Time interleaver (optionally) Frequency interleaver
Dataslices	Number only limited by FPGA size
Bandwidth	freely selectable, only limited by FPGA size
Channel spacing	6, 8 MHz
Guard Interval	1/64, 1/128
Level correction	0dB down to -40dB
Output	 I/Q baseband IF (0 – 70 MHz without steps) DUC (0 – 900 MHz without steps, optionally)
MER	>40dB (precise value depending on the DAC)
Platforms	Altera, Xilinx, Lattice
Language	VHDL
Dependencies	none

