

16ch QAM & DUC FPGA IP-Core



DVB-C Modulation According to ETSI-EN 300 429 V1.2.1 with Digital Upconversion

- QAM Modulation according to ETSI EN 300 429 V1.2.1
- 16 DVB-C channels to 7000 kSym/s max
- Signal quality: MER > 44dB
- Input: MPEG2 transport stream
- Output on AD9739 (or similar DAC)
- Channels can be chosen freely in a frequency range between 50 and 950 MHz
- Output level of each channel can be attenuated individually
- Power consumption ca. 1 Watt / channel
- TS-Processing, modulators and upconversion settable by SPI (or other interfaces at your choice)
- Apart from configuration no CPU support needed
- No dependencies on 3rd-party IP cores or code generators

Hardware Platforms

- Xilinx Virtex 6 / 7
- Xilinx Kintex 7
- Altera Stratix IV / V
- · Altera Arria II / V

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Mail info@maintech.de Web www.maintech.de Digital upconversion is a consequent step on the way to a completely digital signal processing in the transmission of data.

It features the translation of one ore more channels from a baseband signal directly to the required output frequency. Increasing the sample rate, filtering and mixing to achieve the desired carrier frequencies are essential elements of digital upconversion.

Digital upconversion provides a substantially higher signal quality of the different carriers while the output frequency can be chosen freely. This means a compact design of the hardware platform at significantly lower costs.

Performing a DVB-C modulation with completely digital upconversion allows a low power consumption respectively high energy efficiency. All channels can be set and switched on/off individually. The solution is adjacent channel compatible. Excellent MER and shoulder attenuation values are key advantages of maintech's multiple FPGA QAM modulation with DUC.

Short-term evaluation platforms:
Xilinx Virtex-6 LX130T Evaluation Kit by AVNET
Analog Devices AD9739-CMTS-EBZ Evaluation Kit (see fig.)

IP Core

maintech's IP cores are available in different versions, from finished binary images to the complete VHDL source code. The 16ch QAM with DUC IP core was developed with particular attention on the following aspects:

- Flexible configuration depending on available ressources and necessary RF processing
- To compensate for the unavoidable FIFO delay, there are PCR correction and a stuffing packets generator available which raises the transport stream rate to the needed transmission rate
- All transmission parameters can be changed during operation; changes are applied immediately
- Adaptable configuration and data interfaces allow a fast customization to your already existing components or your design

QAM Modulator	
Constellations	QAM16, QAM32, QAM64, QAM128, QAM256
Symbol rate	1000-7000 kSym/s
MER	>44dB
Output	Between 50 and 950 MHz
Level correction	0 down to -10dB
TS input	8 Bit parallel + clock & sync (SPI), PCR correction included

